



Reg. No. :

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Question Paper Code : X 20442

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Electronics and Communication Engineering
EC 6304 – ELECTRONIC CIRCUITS – I
(Regulations 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Why is the operating point selected at the Centre of the active region ?
2. Define Stability factor.
3. What is the need of differential amplifier ?
4. What is meant by bootstrapping ?
5. Determine the output impedance of a JFET amplifier shown in Figure 3. Let $g_m = 2 \text{ mA/V}$ and $\lambda=0$.

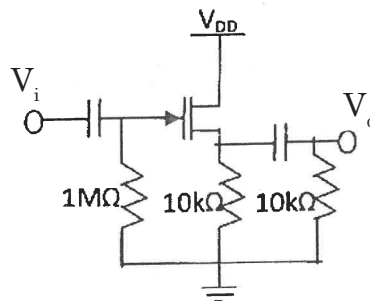


Figure 3

6. Compare between JFET and MOSFET amplifiers.



7. What is the reason for reduction in gain at lower and higher frequencies in case of amplifiers ?
8. Determine the unity-gain bandwidth of a FET with parameters, $C_{gd} = 10 \text{ fF}$, $C_{gs} = 50 \text{ fF}$ and $g_m = 1.2 \text{ mA/V}$.
9. State the advantages of current steering circuit.
10. Define active load and list the types of active load.

PART – B

(5×13=65 Marks)

11. a) i) The parameters for each transistor in the circuit in Figure-5, are $h_{fe} = 100$ and $V_{BE_{on}} = 0.7\text{V}$. Determine the Q-point values of base, collector and emitter currents in Q_1 and Q_2 . (6)

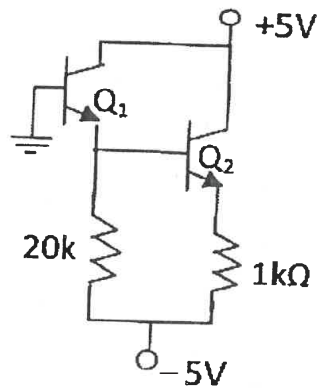


Figure 5

- ii) Determine the change in collector current produced in each bias referred to in Figures 6(a) and 6(b), when the circuit temperature raised from 25°C to 105°C and $I_{CBO} = 15 \text{ nA @ } 25^\circ\text{C}$. (7)

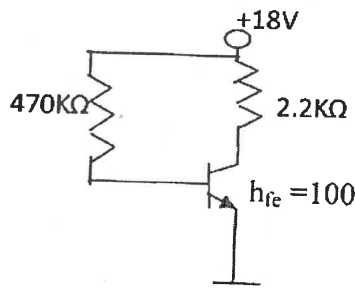


Figure 6(a)

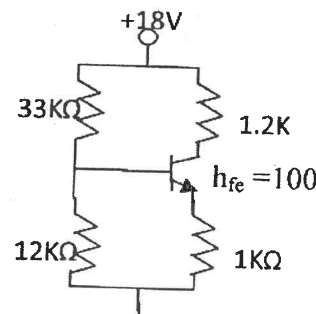


Figure 6(b)

(OR)



- b) i) Determine the quiescent current and voltage values in a p-channel JFET circuit (Vide Figure-7). (4)

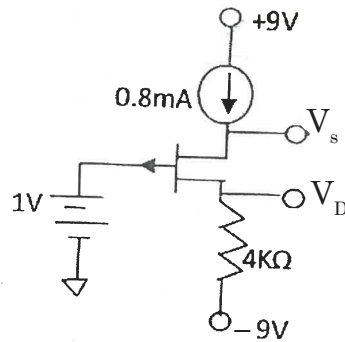


Figure 7

- ii) The circuit in Figure 8, let $h_{fe} = 100$. (1) Find V_{TH} and R_{TH} for the base circuit. (2) Determine I_{CQ} and V_{CEQ} . (3) Draw the DC load line. (9)

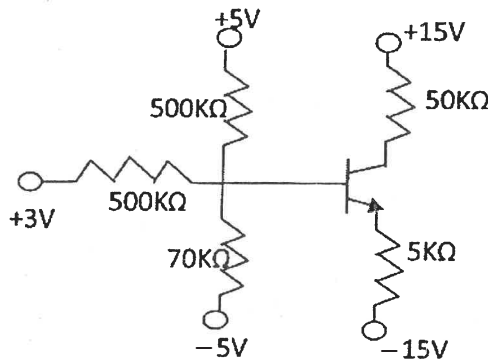


Figure 8

12. a) Draw the a.c equivalent circuit of a CE amplifier with voltage divider bias and derive the expression for current gain, voltage gain, Input impedance, output admittance and overall current gain. (13)

(OR)

- b) Explain the operation of cascade amplifier and derive Voltage gain, overall input Resistance overall current gain and output impedance. (13)

13. a) i) Draw the small signal equivalent circuit of NMOS source follower. Also obtain the expression for the gain. (8)

- ii) With relevant circuit diagram, explain cascode NMOS amplifier circuit. (5)

(OR)



- b) Determine the small-signal voltage gain of a JFET amplifier. Consider the circuit shown in Figure 9 with transistor parameters : $I_{DSS} = 12 \text{ mA}$, $V_P = -4 \text{ V}$ and $\lambda = 0.008 \text{ V}^{-1}$. Also draw the Small-signal equivalent circuit of common source JFET, assuming bypass capacitor acts as a short circuit. (13)

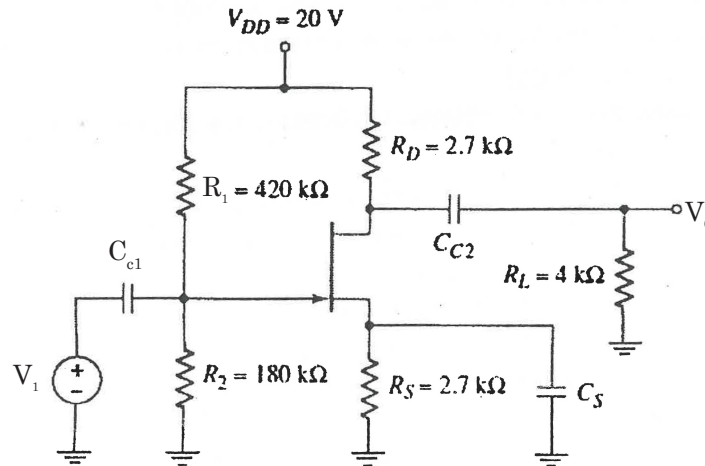


Figure 9

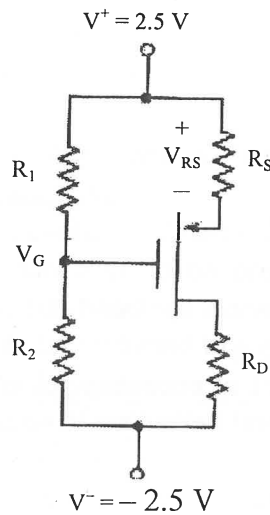
14. a) With neat sketch explain hybrid π CE transistor model. Derive the expression for various components in terms of 'h' parameters.
(OR)
b) Explain the high frequency analysis of JFET with necessary circuit diagram and gain bandwidth product.
15. a) Draw and explain the operation of a simple MOSFET amplifier with active load and derive its voltage gain using small-signal equivalent circuit.
(OR)
b) With necessary diagrams, explain the operation of a CMOS differential amplifier. Using small signal analysis, derive the expression for its voltage gain.



PART – C

(1×15=15 Marks)

16. a) Design the circuit given below such that $I_{DQ} = 100 \mu A$, $V_{SDQ} = 3V$ and $V_{RS} = 0.8V$. Note that V_{RS} is the voltage across the source resistor R_s . The value of the larger bias resistor, either R_1 or R_2 is to be $200 k\Omega$. Transistor parameter values are $K_p = 100 \mu A/V^2$ and $V_{TP} = -0.4 V$. The conduction parameter, K_p may vary by ± 5 percent.



(OR)

- b) Design the cascode circuit shown below to meet the following specifications : $V_{CE1} = V_{CE2} = 2.5 V$, $V_{RE} = 0.7 V$, $I_{C1} \cong I_{C2} \cong 1mA$, and $I_{R1} \cong I_{R2} \cong I_{R3} = 0.10 mA$.

